

## Abstract

In a memory and/or data processing device having at least two stacked layers which are supported by a substrate or forming a sandwich self-supporting structure, wherein the layers comprise memory and/or processing circuitry with mutual connections between the layers and/or to circuitry in the substrate, the layers are mutually arranged such that contiguous layers form a staggered structure on at least one edge of the device and at least one electrical edge conductor is provided passing over the edge on one layer and down one step at a time, enabling the connection to an electrical conductor in any of the following layers in the stack. A method for manufacturing a device of this kind comprises steps for adding said layers successively, one layer at a time such that the layers form a staggered structure and for providing one or more layers with at least one electrical contacting pad for linking to one or more interlayer edge connectors.

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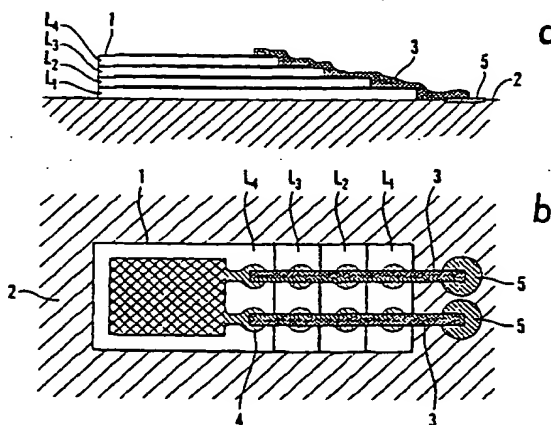
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(54) Title: VERTICAL ELECTRICAL INTERCONNECTIONS IN A STACK



(57) Abstract: In a memory and/or data processing device having at least two stacked layers which are supported by a substrate or forming a sandwich self-supporting structure, wherein the layers comprise memory and/or processing circuitry with mutual connections between the layers and/or to circuitry in the substrate, the layers are mutually arranged such that contiguous layers form a staggered structure on at least one edge of the device and at least one electrical edge conductor is provided passing over the edge on one layer and down one step at a time, enabling the connection to an electrical conductor in any of the following layers in the stack. A method for manufacturing a device of this kind comprises steps for adding said layers successively, one layer at a time such that the layers form a staggered structure and for providing one or more layers with at least one electrical contacting pad for linking to one or more interlayer edge connectors.

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